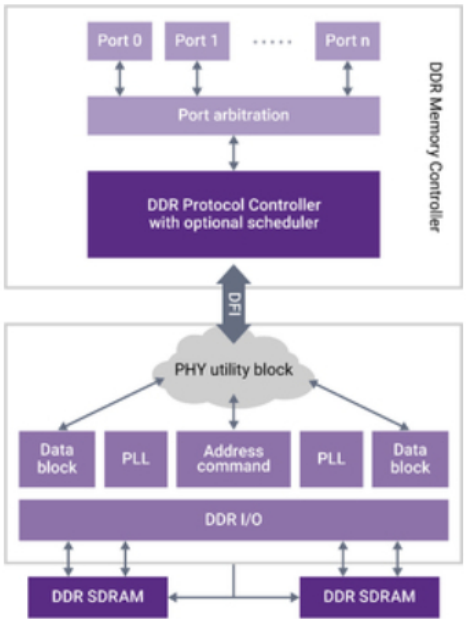
SYNOPSYS

DesignWare DDR IP Solutions



Overview

The DesignWare® DDR Memory Interface IP provides complete system-level IP solutions for SoCs requiring an interface to one or a range of high-performance DDR5, DDR4, DDR3/3L, DDR2, LPDDR5, LPDDR4/4X, LPDDR3, LPDDR2, LPDDR, HBM2 and HBM2E SDRAMs or memory modules (DIMMs). Optimized for high data bandwidth, low power and enhanced signaling features, the complete DesignWare DDR Memory Interface IP solution includes a choice of scalable digital controllers, an integrated hard macro PHY delivering memory system performance of up to 6400 Mbps, and verification IP. There are several Synopsys DesignWare DDR PHY IP cores to choose from, as detailed in the table below.

Most of the DFI-compatible DDR PHYs are supported by Synopsys' unique DesignWare DDR PHY Compiler. Synopsys' DesignWare DDR5/4 Controller, LPDDR5/4/4X Controller, and Enhanced Universal DDR Memory and Protocol Controller IP feature a DFI-compliant interface, low latency and low gate count while offering high bandwidth. Optional market-specific features like AMBA AXI/4 AXI Quality of Service (QoS) and Reliability, Availability and Serviceability (RAS) features allow you to match the area and capabilities of the controllers to your needs.

Synopsys also offers DesignWare HBM2/HBM2E IP, which provides 14x the bandwidth of DDR4 IP and ten times better power efficiency for graphics, high-performance computing, and networking SoCs.

Meet Your DDR5 and LPDDR5 IP Needs!

With the silicon-proven DesignWare DDR5 and LPDDR5 IP solutions offering differentiated features for a wide range of applications, including high-performance computing, mobile, and automotive

Learn more

PRODUCTS

DDR5 +

DDR4 +

LPDDR5 +

LPDDR5/4/4X Controller

LPDDR5/4/4X PHY

Interface IP Subsystems

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IP Overview Brochure

IP Accelerated Brochure

NEWS

Synopsys Demonstrates Silicon Proof of DesignWare 112G Ethernet PHY IP in 5nm Process

Industry's First IDE Security IP Modules for PCIe 5.0 and CXL 2.0

Synopsys & Socionext to Deploy HBM2E IP for 5-nm Process in AI & HPC SoCs

WEBINARS

Ensuring Known Good Dies in SiPs with Die-to-Die PHY IP

Reducing Latency in Cloud Computing SoCs: CXL, CCIX and PCIe IP

AI SoC Case Study: Emerging Neural Networks Drive IP Innovation

EVENTS

ARC Processor Virtual Summit – Now Available On-Demand.

IP SoC Conference 2020

VIDEOS

Data Overload In The Data Center

Product Update: Silicon-Proven Automotive-Grade DesignWare IP

DDR3/3L/3U +

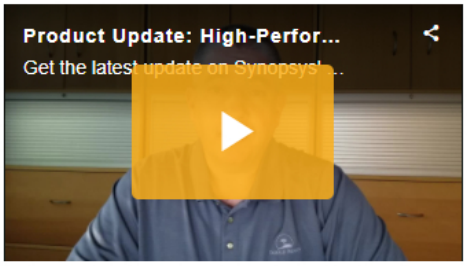
DDR2 +

LPDDR/mDDR +

Verification IP

LPDDR2 +

HBM2/HBM2E ›



Product Update: High-Performance DesignWare Memory Interface IP

Get the latest update on Synopsys' DesignWare Memory Interface IP for DDR5, LPDDR5, and HBM2/2E.

Watch now

DesignWare DDR PHY	SDRAMs Supported / Maximum Data Rate	Interface to Memory Controller	Typical Application
LPDDR5/4/4X PHY	LPDDR5 / 6400 Mbps LPDDR4 / 4267 Mbps LPDDR4X / 4267 Mbps	DFI 5.0	Design in 16-nm and below that requires high-performance mobile SDRAM support up to 6400 Mbps
DDR5/4 PHY	DDR5 / 6400 Mbps DDR4 / 3200 Mbps	DFI 5.0	Design in 16-nm and below that requires high-performance DDR5/4 support up to 6400 Mbps
DDR4/3 PHY	DDR4 / 3200 Mbps DDR3 / 2133 Mbps DDR3L / 2133 Mbps	DFI 4.0	Design in 28-nm and below that requires high-performance DDR4/3 support up to 3200 Mbps
LPDDR4 multiPHY	LPDDR4 / 4267 Mbps LPDDR3 / 2133 Mbps DDR4 / 3200 Mbps DDR3 / 2133 Mbps DDR3L / 2133 Mbps	DFI 4.0	Design in 28-nm and below; that requires high-performance mobile SDRAM support (LPDDR4/3) up to 4267 Mbps and/or high-performance DDR4/3 support up to 3200 Mbps for small memory subsystems.
DDR4 multiPHY	DDR4 / 2667 Mbps DDR3 / 2133 Mbps DDR3L / 1866 Mbps LPDDR2 / 1066 Mbps LPDDR3 / 2133 Mbps	DFI 3.1	Design in 28-nm and below that requires high-performance DDR4/3 support up to 2667 Mbps and/or high-performance mobile SDRAM support (LPDDR3/2) up to 2133 Mbps.
Gen2 DDR multiPHY	DDR3 / 2133 Mbps DDR3L / 1866 Mbps LPDDR2 / 1066 Mbps LPDDR3 / 2133 Mbps	DFI 3.1	Design in 28-nm and below that requires high-performance mobile SDRAM support (LPDDR3/2) up to 2133 Mbps and/or high-performance DDR3 support up to 2133 Mbps.
DDR3/2 SDRAM PHY	DDR3 / 2133 Mbps DDR3L / 1600Mbps DDR2 / 1066 Mbps	DFI 2.1	Design in 65 - 28-nm that requires high-performance DDR3 up to 2133 Mbps.
DDR multiPHY	DDR3 / 1066 Mbps	DFI 2.1	Design in 65 - 28-nm that requires DDR3 and/or

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	DDR3L / 1066Mbps DDR2 / 1066 Mbps LPDDR / 400 Mbps LPDDR2 / 1066 Mbps		DDR2 support up to 1066 Mbps along with LPDDR/LPDDR2 support.